Base Resistance Contributions in SiGe HBT Devices

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Outline

Base Resistance Contributions in SiGe HBT Devices

- Motivation - *why it is important to accurately determine R_B*
- Components of the base resistance – *how to partition R_B*
- Dual base tetrode device – *description of test structure*
- Measurement conditions – *how to perform on wafer measurements*
- Extraction method – *how to obtain R_B and its components*
  - Extraction results using recent bipolar technology – *application to B5T*
- Process split results and variation – *encountered errors & statistics*
- Extraction results using TCAD simulation – *method robustness*
- Conclusion

Motivation

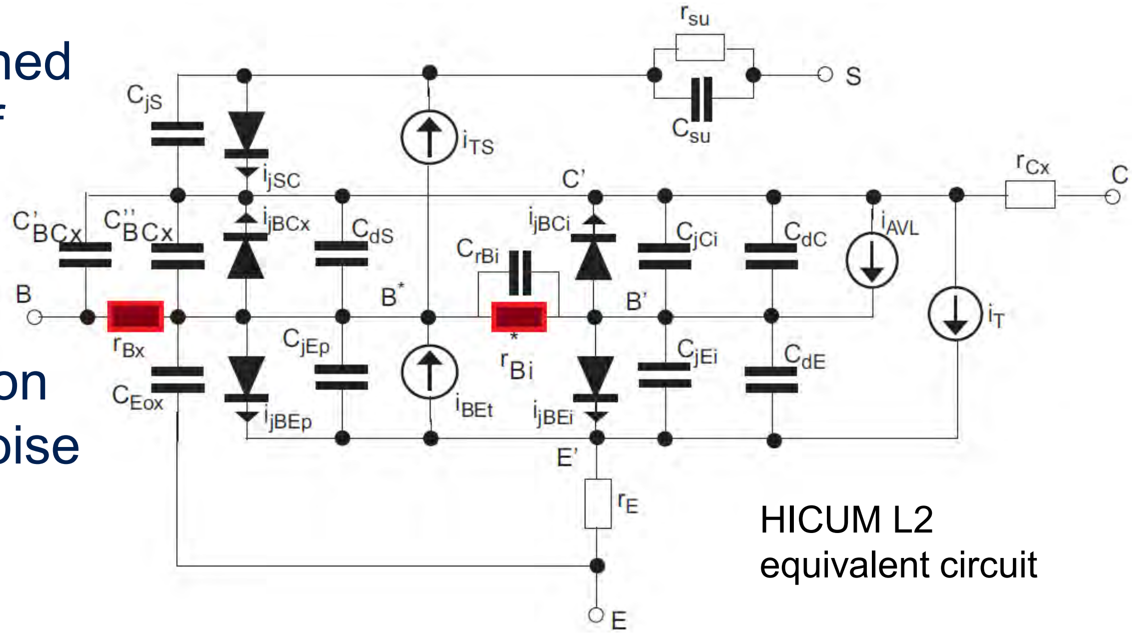
why it is important to accurately determine R_B

- resistances to be determined before model extraction of currents and AC characteristics

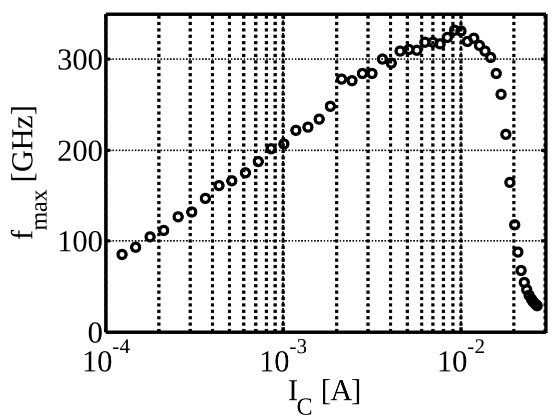
- R_B has significant impact on device speed (f_{max}) and noise behaviour (NFmin)

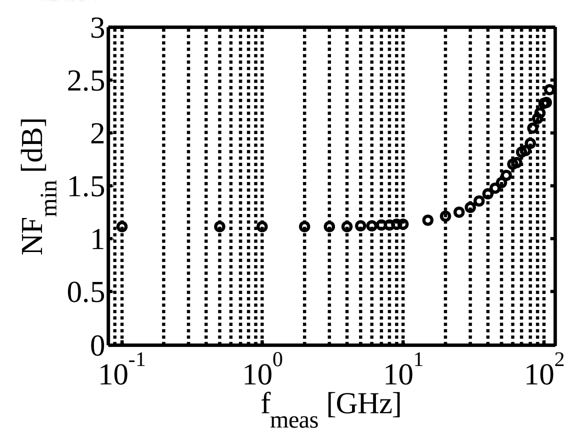
$$f_{\max} \approx \sqrt{\frac{f_T}{8\pi R_B C_{BC}}}$$

\w $$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$



HICUM L2 equivalent circuit

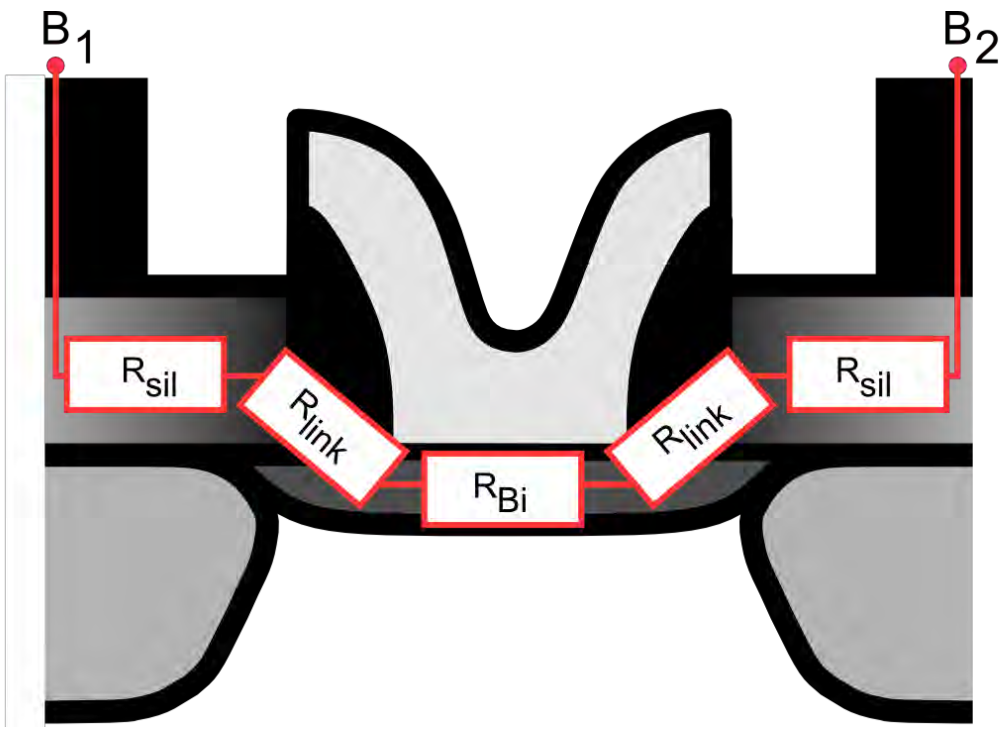




Components of the base resistance

how to partition R_B

- base resistance is composed of the intrinsic base resistance R_{Bi} and the extrinsic base resistance R_{Bx}
- intrinsic: bias dependent internal base sheet resistance r_{SBi}
- extrinsic: from the inner base (emitter window edge) to the base contact
  - including involved contact resistance (base link region) below the spacer

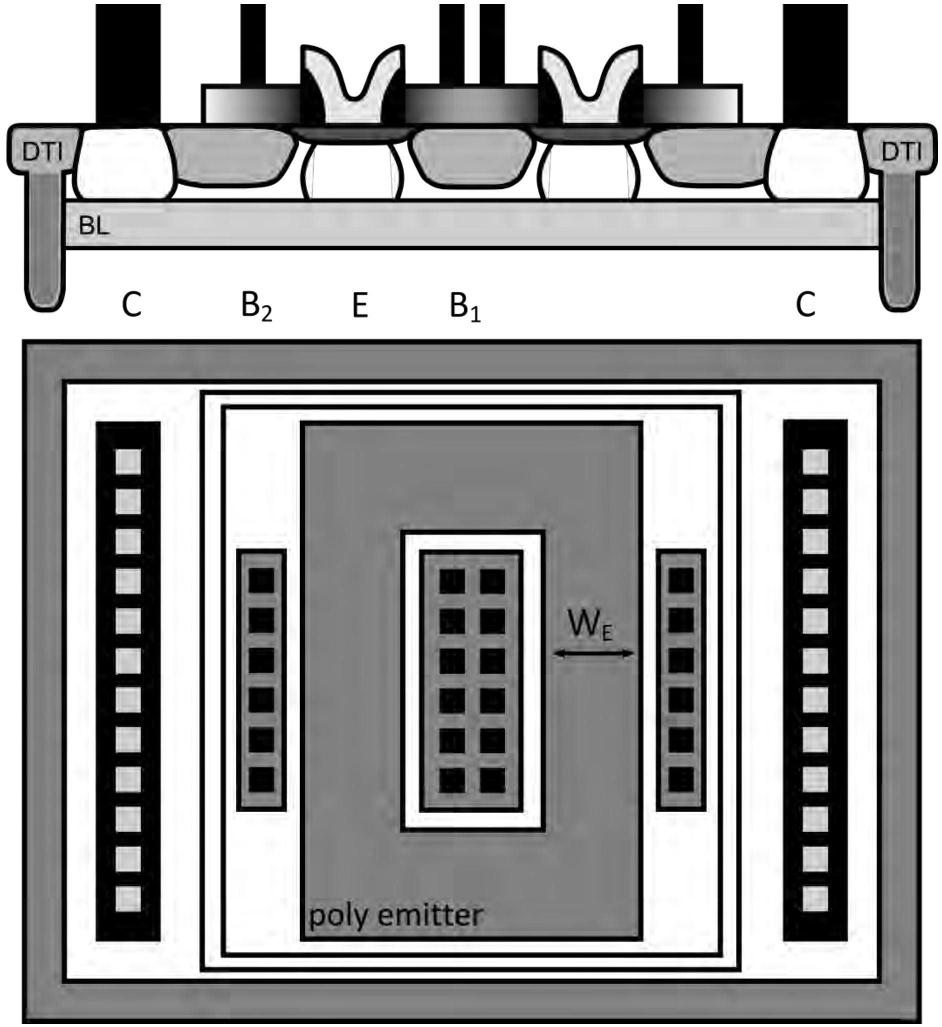


Cross section of SiGe SEG HBT with R_B contributions

Dual base tetrode device

description of test structure

- dual base test structures present an improved approach compared to classical pinch-resistor structures (as presented in [1])
- extract the sheet resistance value of each component using simple yet accurate DC measurements
- two base terminals B1 and B2 independently accessible
- ring emitter structure to electrically separate the two bases



cross section & top view of the dual base tetrode

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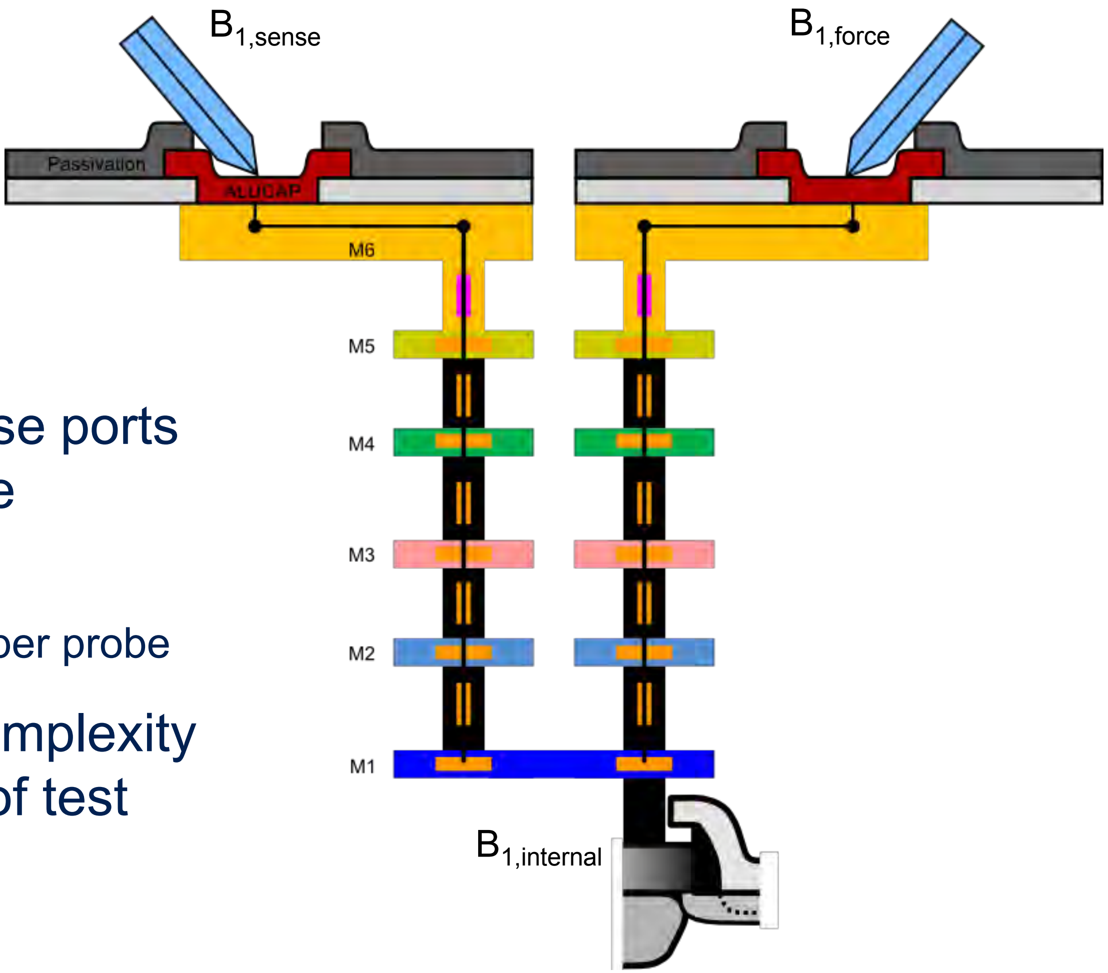
Dual base tetrode device

description of test structure

- improvements over the original device structure include kelvin type connection to cancel out contact resistances
- independent force and sense ports shorted in M1 layer improve measurement accuracy
  - usually >2Ω contact resistance per probe
- increased measurement complexity using 6 probes for biasing of test structure

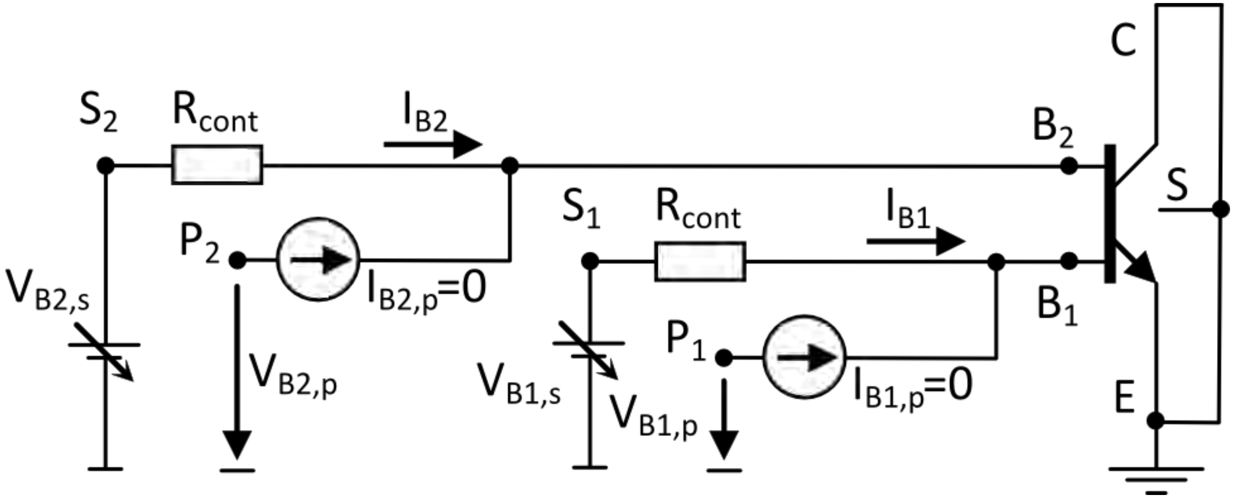


metal stack up to probe connection on aluminum pads

Dual base tetrode device

description of test structure

- simplified equivalent circuit due to kelvin type connection

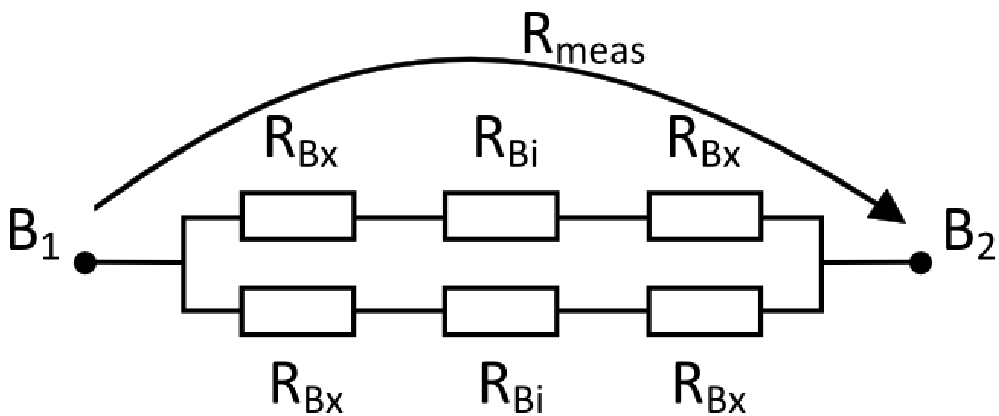


equivalent circuit of tetrode structure with individual base contacts

- resistance contributions measured suitable for xtr

$$R_{meas} = \frac{V_{B2,p} - V_{B1,p}}{(|I_{B1}| + |I_{B2}|)/2}$$

$$= R_{Bx} + R_{Bi}/2$$



resistance contributions measured between B1 and B2

Measurement conditions

how to perform on wafer measurements

- forcing probe (P) ports to zero current to ensure proper kelvin measurement and measurement of applied bias at M1 level
- differential bias applied on force port with constant ΔV_B (40mV)

$$\Delta V_B = V_{B2,s} - V_{B1,s}$$

- bias conditions for V_{BE}: -0.5 .. 0.5V
  - avoid breakdown in reverse bias
  - avoid active BE junction in forward mode
- measured resistance calculated using voltage of floating probes (P)

$$R_{meas} = \frac{V_{B2,p} - V_{B1,p}}{(|I_{B1}| + |I_{B2}|)/2} \quad \backslash w\ I_{probe} = 0$$

- the two contributions measured in each structure (R_{Bi} and R_{Bx}) are best seen in the equivalent circuit (two parallel series resistances)

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Extraction method

how to obtain R_B and its components

- extraction is based on geometry scaling approach
- R_{Bx} is assumed to be constantfor a variation of the device length and independent of bias conditions [$R_{Bx} = f(l_E)$]
- intrinsic base resistance is a function of all factors [$R_{Bi} = f(w_E, l_E, V_{BE})$]

$$R_{meas}^{i,j,k} = R_{Bx}(l_E^j) + \frac{R_{Bi}(w_E^i, l_E^j, V_{BE}^k)}{2}$$ as in [2]

- two lengths per emitter width structure to cancel out the corner effects
- subtraction of the current of two structures gives the current of a inner, two-dimensional structure with an effective device length of Δl_E

$$R_{meas}^{i,j,k} \cdot \Delta l_E = \frac{R_{sBi}(V_{BE}^k) \cdot (w_E^i - 2d)}{2} + R_{Bx} \cdot \Delta l_E$$

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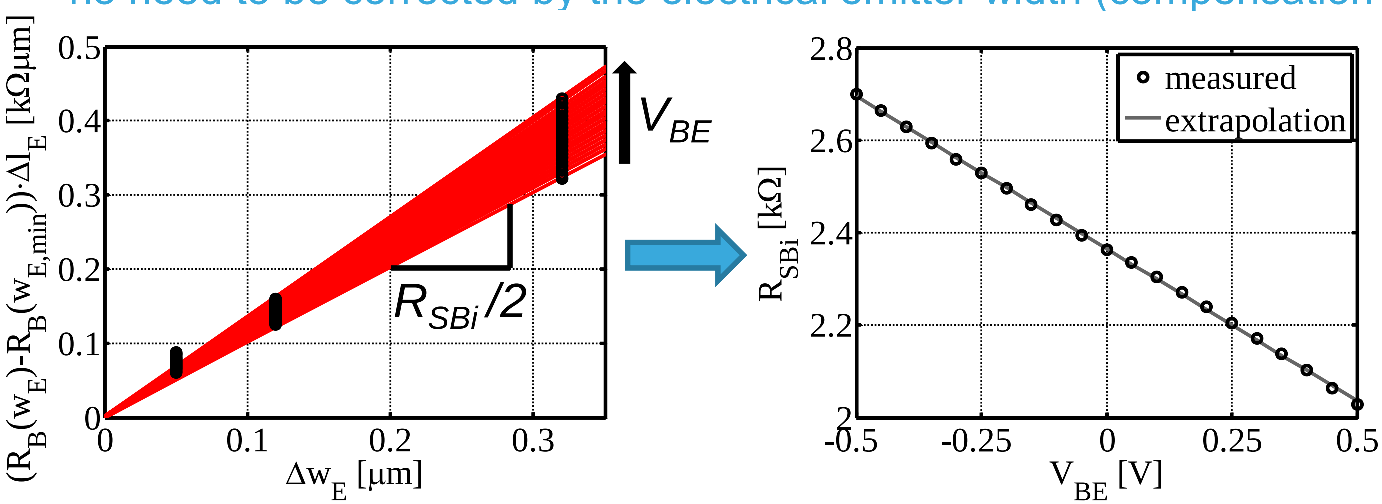
Extraction method

how to obtain R_B and its components

- $R_{meas}\Delta l_E$ curve may be normalized by a w_E reference structure
- smallest w_E structure used for suppression of undesired corner effects
- deduction of this reference yields a corrected $\Delta_{lw}R_{meas}$ normalized by Δl_E versus a relative emitter width Δw_E
  - no need to be corrected by the electrical emitter width (compensation by d)



  - linear regression must cross the origin

$$\Delta_{lw}R_{meas}^{i,j,k}\cdot\Delta l_E = \frac{R_{SBi}(V_{BE}^{k})\cdot\Delta w_E}{2}$$

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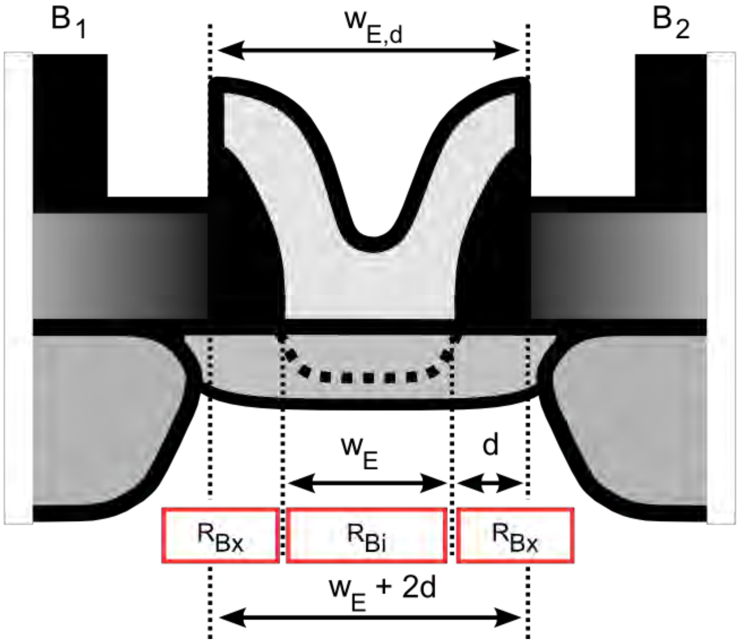
Extraction method

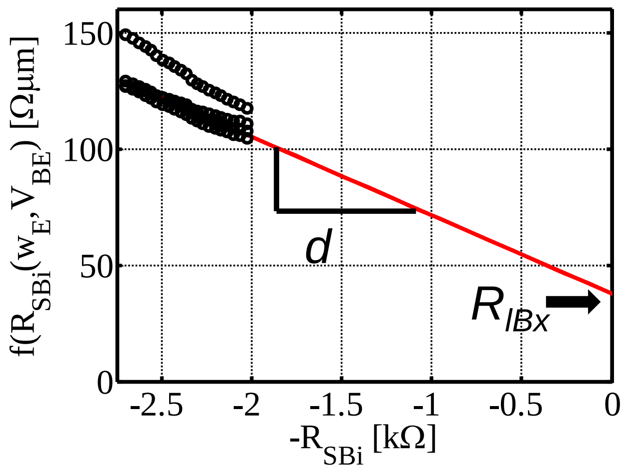
how to obtain R_B and its components

- compensate for parasitic corner effects and layout by electrical intrinsic base resistance width with $w_{E,eff} = w_{E,d} - 2d$
- extraction from normalized measured base resistance versus negative bias dependent internal base resistance

$$f(R_{SBi}) = R_{SBi}(V_{BE}^{k}) \cdot d + R_{LBx} = \ldots$$

$$\ldots = \Delta_l R_{meas}^{i,j,k} \Delta l_E - R_{SBi}(V_{BE}^{k}) \cdot w_E / 2$$





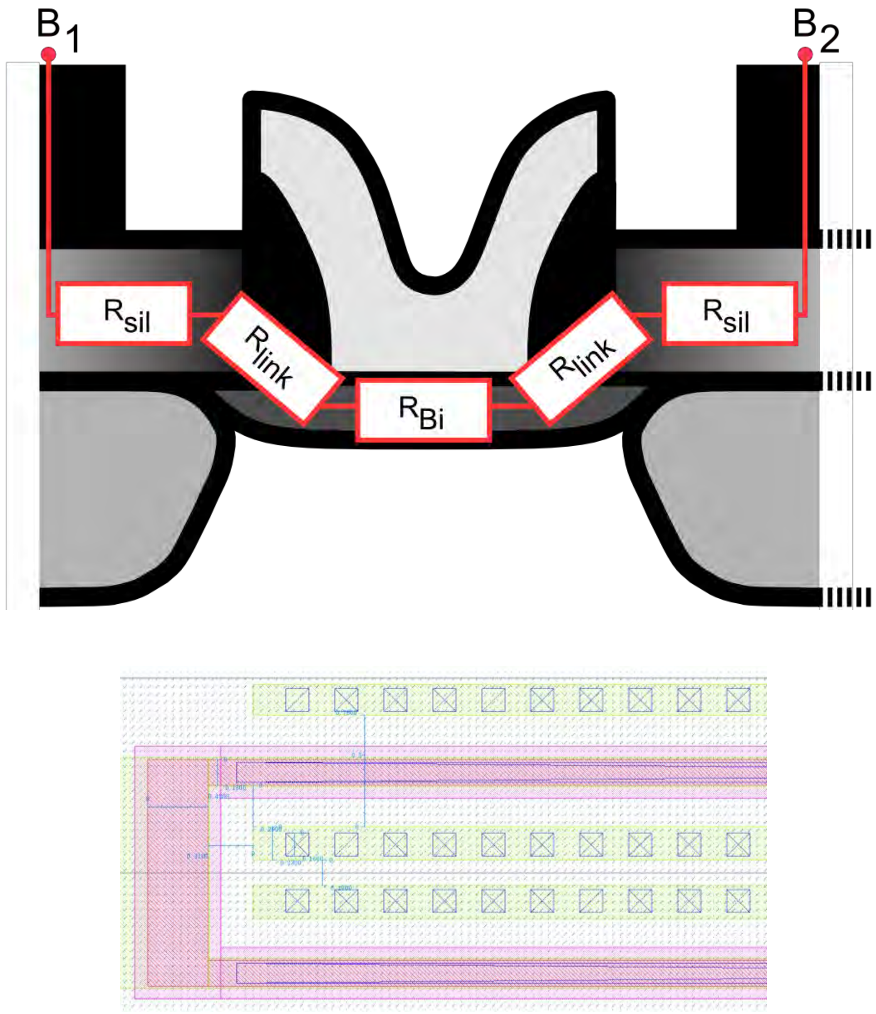
R_{SBi0} [kΩ]	d [nm]	R_{lBx} [Ω·μm]
2.37	-35.6	36.8

→ actual emitter window bigger than drawn emitter window

Extraction method

how to obtain R_B and its components

- external resistance contributions to determine:
  - silicided external base region: R_{sil}
  - base-link region below spacer: R_{link}
- partitioning of external contribution using information from DRM and layout
  $R_{Bx} = R_{sil} + R_{link}$
- DRM process information:
  sheet resistance of silicided 10Ω/□
- w_{sil} = 335nm (from layout)

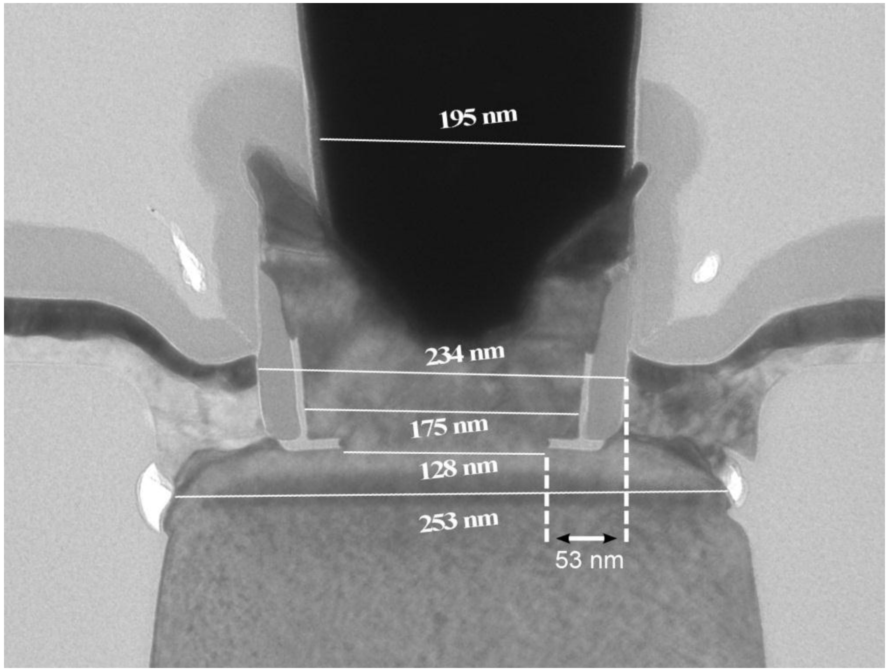


cross section & layout view of tetrode

Extraction method

how to obtain R_B and its components

- determining spacer information from TEM imaging w_{link}=53nm
- $R_{l,link} = R_{lBx} - R_{l,sil} = 33.45\Omega\mu m$
- $R_{slink} = 631\Omega/\square$
- supplemental information from TEM imaging for device simulation:
  - difference of drawn dimensions and actual dimensions on silicon of process



cross section of SiGe HBT with w_E = 0.18µm obtained from TEM imaging analysis

Process split results and variation

encountered errors & statistics

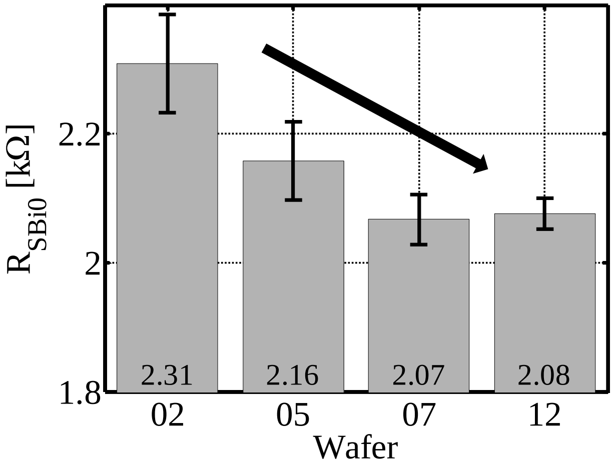
- extrapolation of the extrinsic base resistance times unit length R_{LBx} as well as the geometry correction *d* is performed far from the origin
- small measurement errors or abnormalities in geometry scaling may yield unphysical extraction results
- idea to study the impact of die-to-die variation and quantify uncertainty caused by the extraction routine
- technology parameter variation in process split served for trial
  - measurement and automated extraction on 42 dies per process split

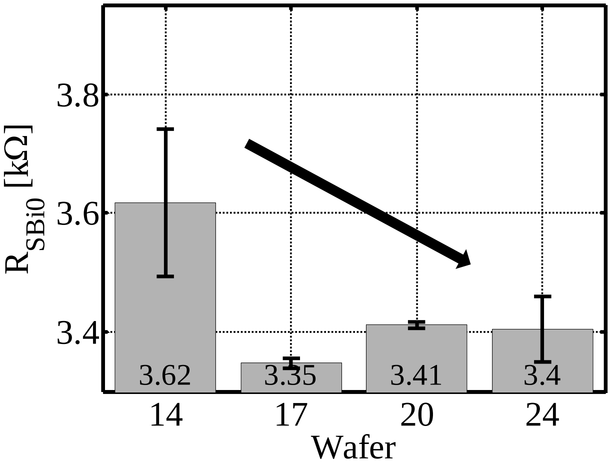
Base width	5nm (reference)			
T_{anneal} [°C]	-	1010	1025	1040
Wafer	W02	W05	W07	W12
Base width	3nm (thin base)			
T_{anneal} [°C]	-	1010	1025	1040
Wafer	W14	W17	W20	W24

Process split results and variation

encountered errors & statistics

- measurement and automated extraction on 42 dies per process split
  - average value with the standard deviation for each wafer



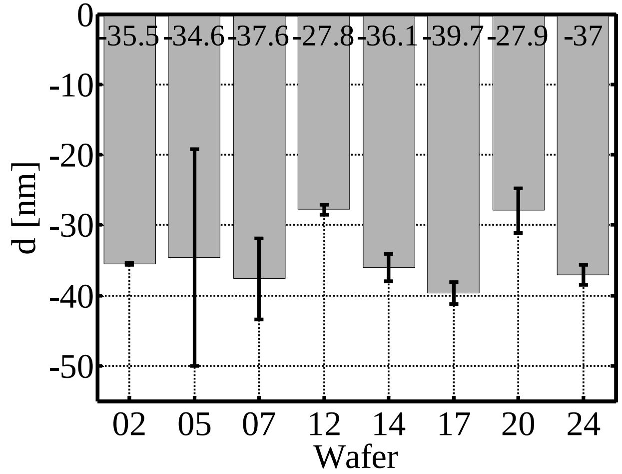


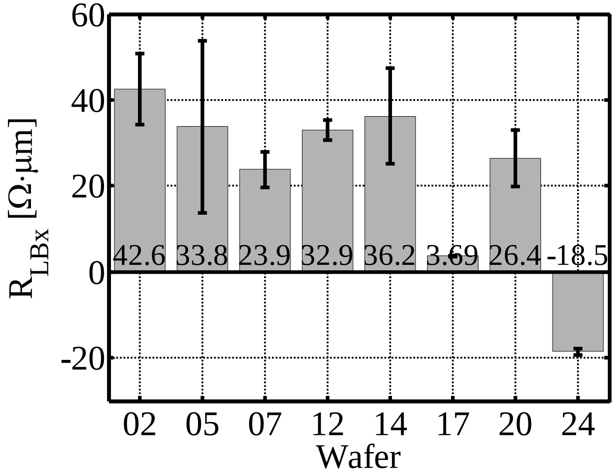
- extracted zero-bias base sheet resistance (R_{SBi0}) is found to be highly increased for the thin base profile
- determination of R_{SBi} seems robust and yields feasible results

Process split results and variation

encountered errors & statistics

- questionable results obtained for geometry correction and extrinsic base resistance R_{LBx}



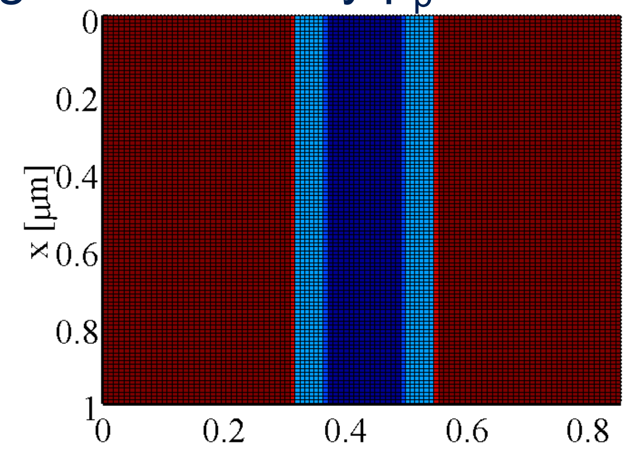


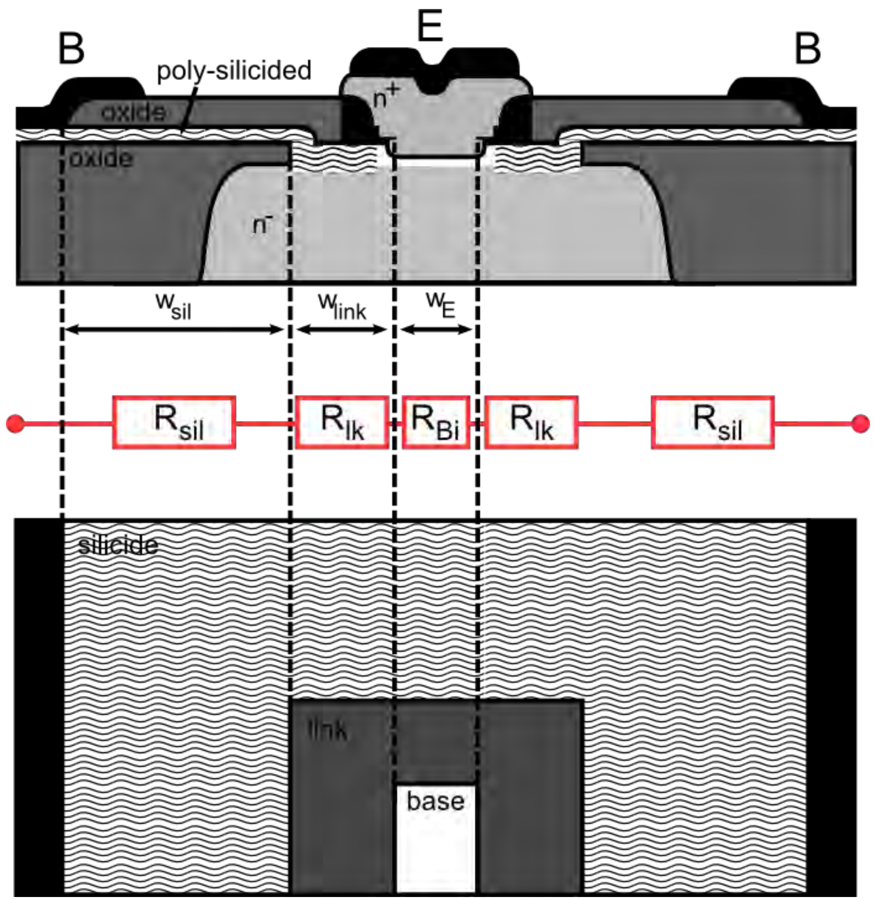
  - possibility of unphysical (negative) resistance value

Extraction results using TCAD simulation

method robustness

- 1D numerical device simulation of tetrode structures [3]
- device structure according to layout combined with additional information on spatial dimensions from TEM imaging
- variable sheet resistance modeled through hole mobility μ_p





cross section & top view of one side of the tetrode

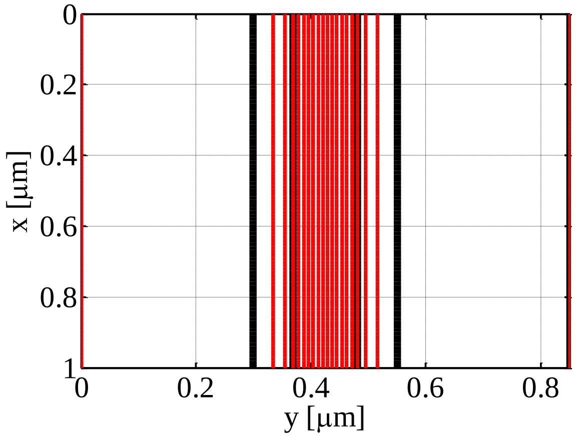
Extraction results using TCAD simulation

method robustness

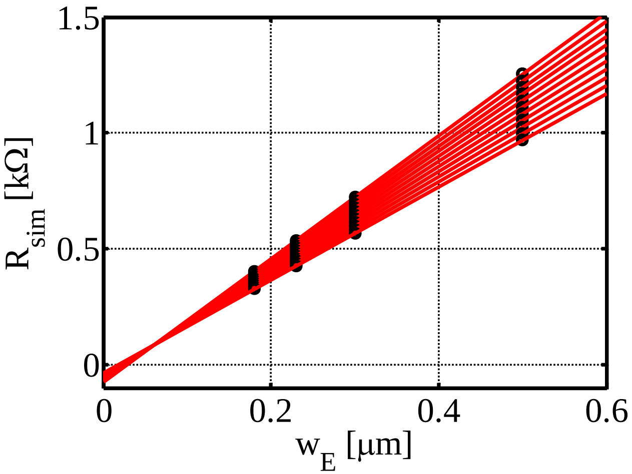
- simulation vs. bias for different device geometries according to silicon specifications of B5T device generation
- application of extraction routine to simulated data
- structure simulated with extracted average values of process split W02

R_{SBi0} [kΩ/□]	R_{Ssil} [Ω/□]	R_{Slink} [Ω/□]
2.37	10	740

- first trial with given electrical dimensions from DRM [$w_{E,d}$ = 0.18, 0.23, 0.3, 0.5 µm]



equipotential lines

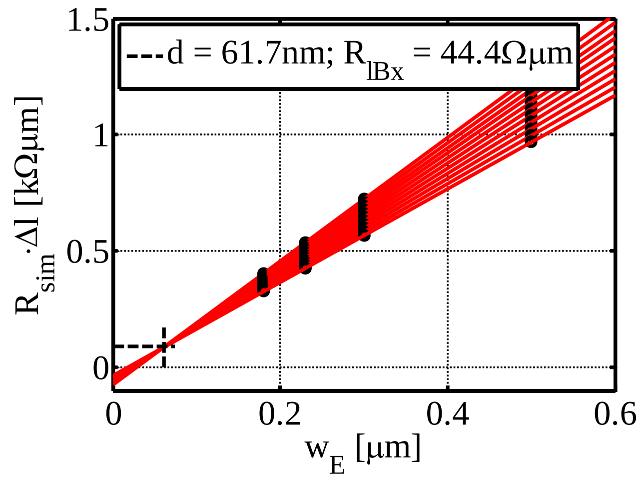


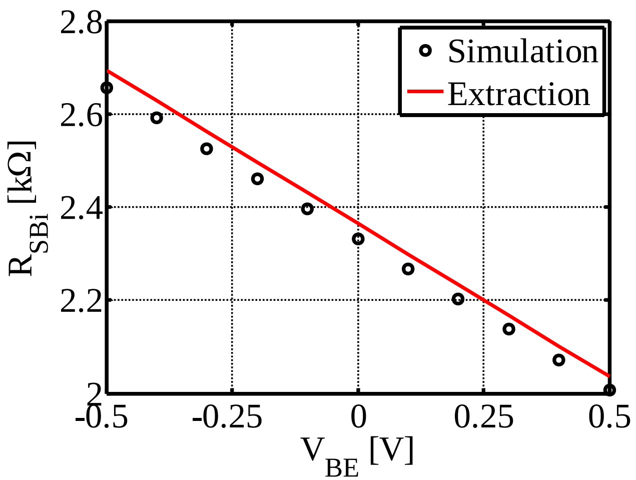
Extraction results using TCAD simulation

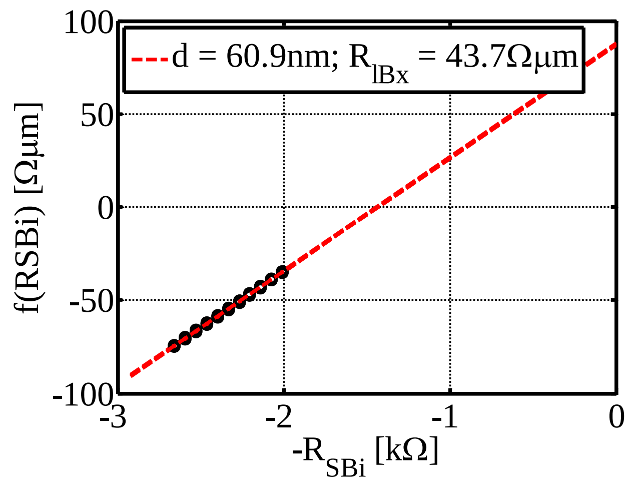
method robustness

- extraction result yields expected quantities:

	R_{SBi0} [kΩ]	d [nm]	R_{lBx} [Ω·μm]
input	2.37	53	42
xtr	2.33	61	44





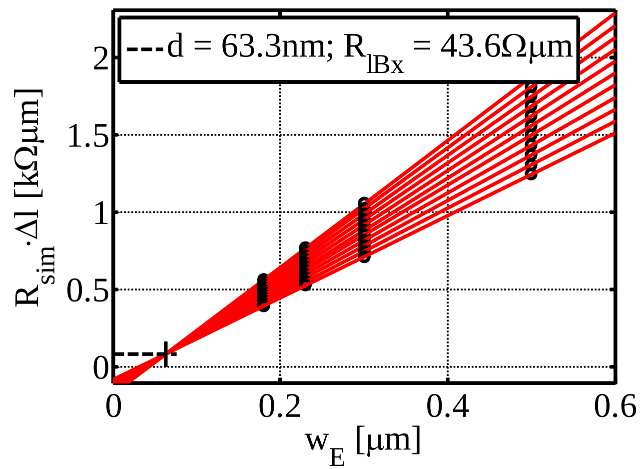


Extraction results using TCAD simulation

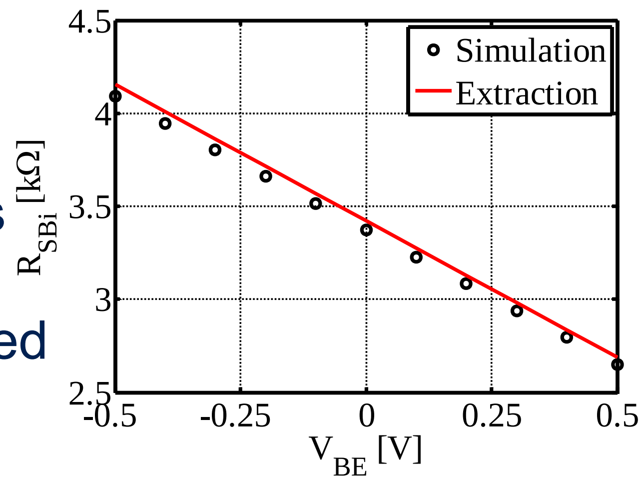
method robustness

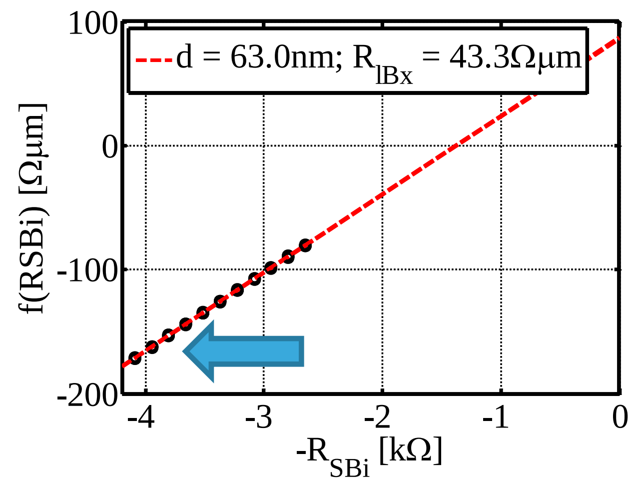
- extraction result for case of W14:

	R_{SBi0} [kΩ]	d [nm]	R_{lBx} [Ω·μm]
input	3.42	53	42
xtr	3.37	63	43



- even though the R_{SBi0} value is about 50% larger (thus further from the origin) the extraction result is in accordance with the expected results



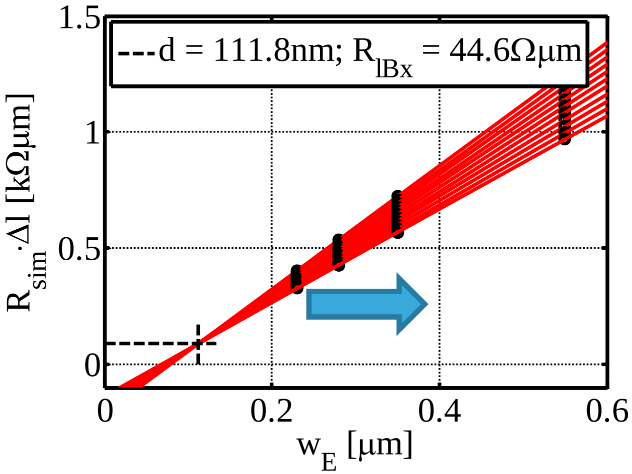


Extraction results using TCAD simulation

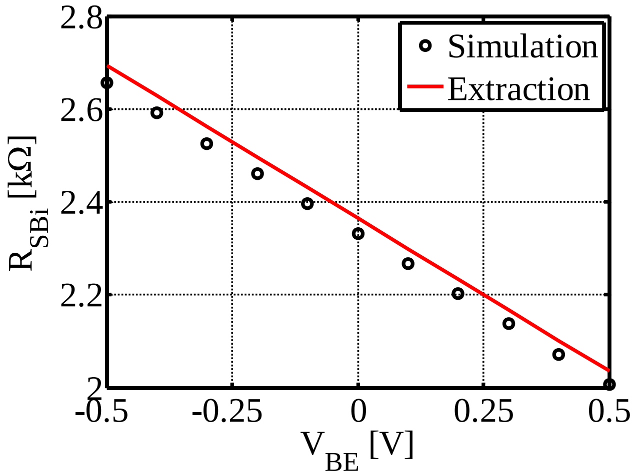
method robustness

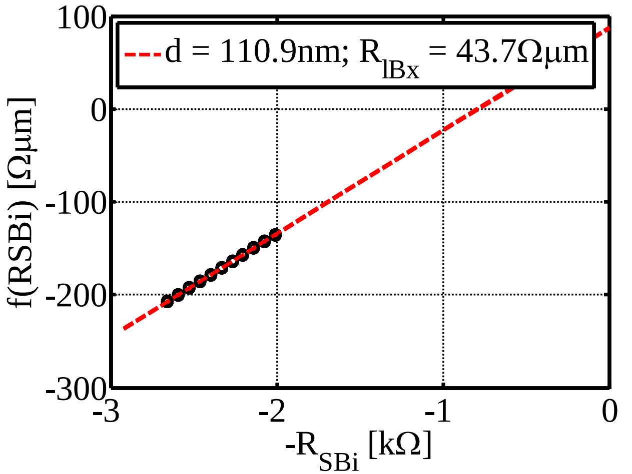
- wrong measure for emitter window width w_E
  - constant offset of Δw_E = 50nm

	R_{SBi0} [kΩ]	d [nm]	R_{lBx} [Ω·µm]
input	2.37	53	42
xtr	2.33	111	44



- method efficiently corrects the emitter window width difference that was added intentionally
- no impact on R_{SBi0} value



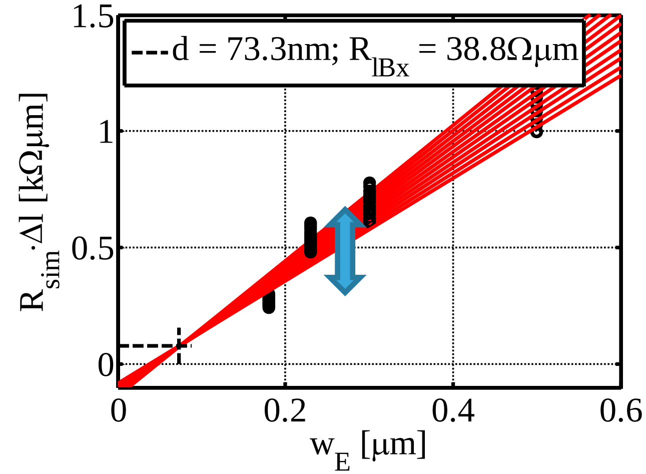


Extraction results using TCAD simulation

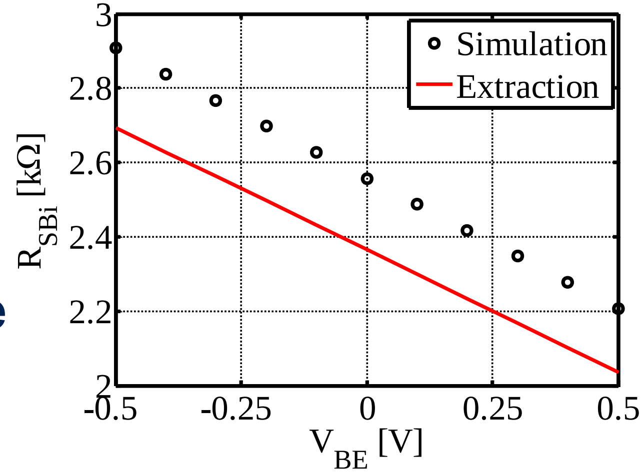
method robustness

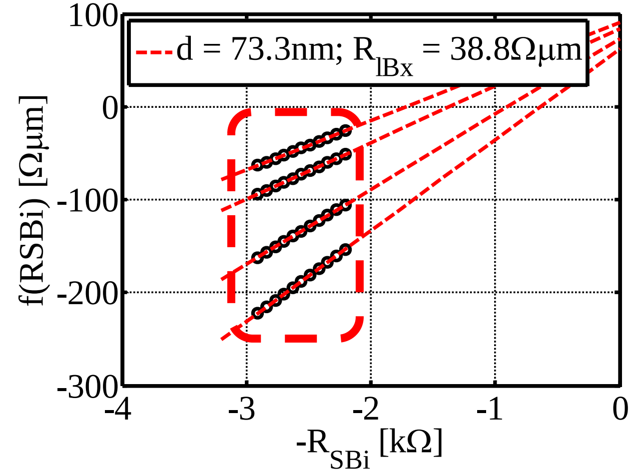
- Random variation of measured resistance
  - intentionally induced 'noise' on R_{meas}

	R_{SBi0} [kΩ]	d [nm]	R_{lBx} [Ω·µm]
input	2.37	53	42
xtr	2.56	73.3	39



- f(RSBi) vs. $-R_{SBi}$ curves not superimposed anymore
- impact on emitter window width extraction as well as R_{SBi0} value

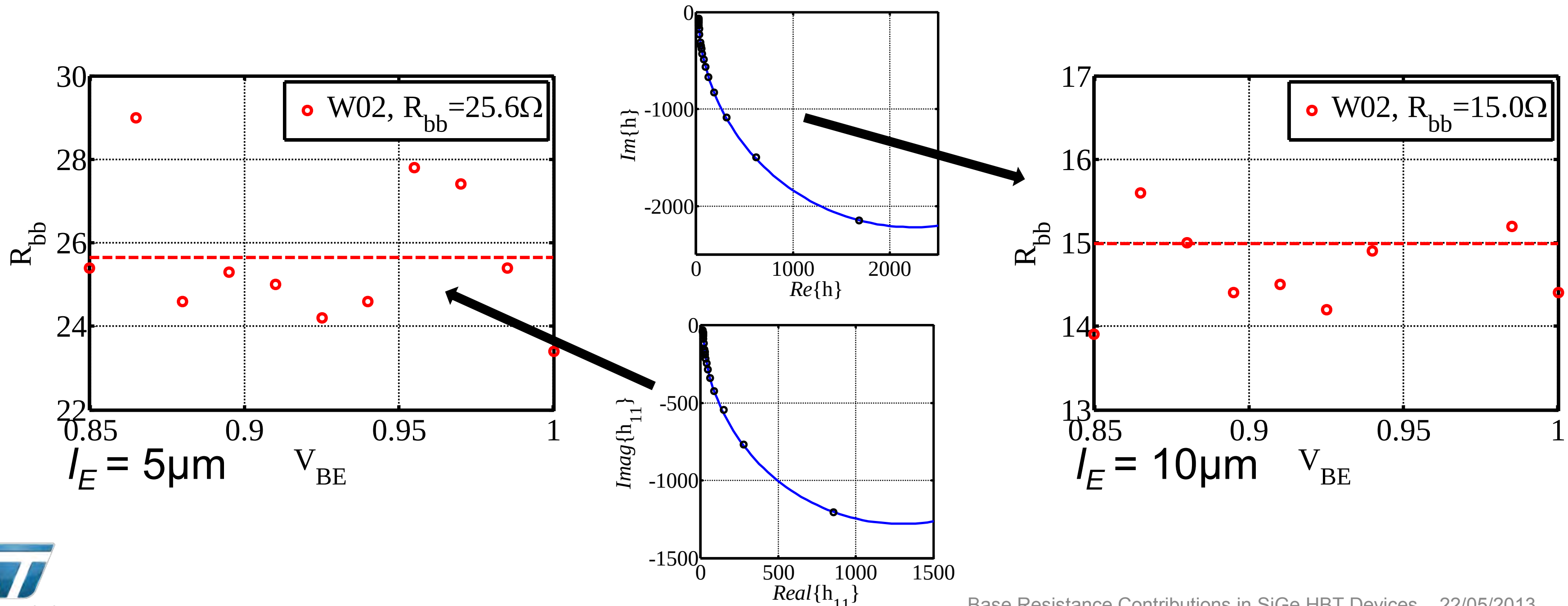




Extraction results using TCAD simulation

method robustness

- simulation of 2D device structure to compare results with RB extraction from semi-circle method [4, 5, 6] on RF msmt structure for w_E = 0.18µm and l_E = 5µm as well as l_E = 10µm
- limited resolution of S-parameter based approach
  - impact of self heating at high current to be taken into account [T↑ => R↑]

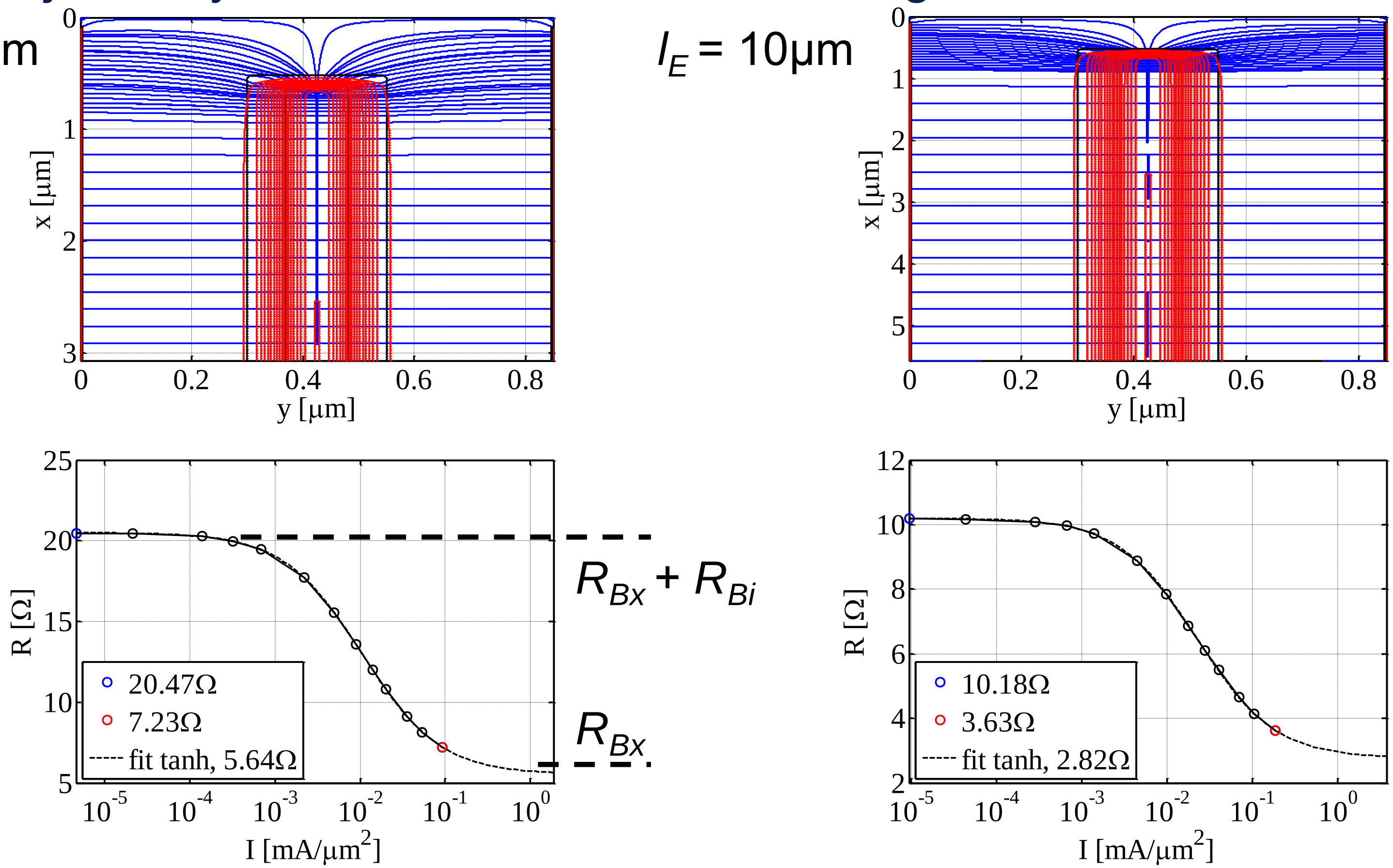


Extraction results using TCAD simulation

method robustness

- total base resistance obtained from simulation of 2D device structure in low injection yields feasible results for both geometries

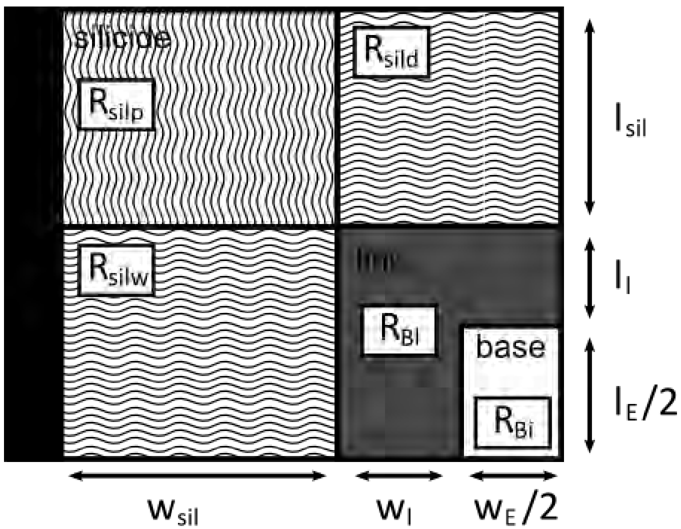
l_E = 5µm

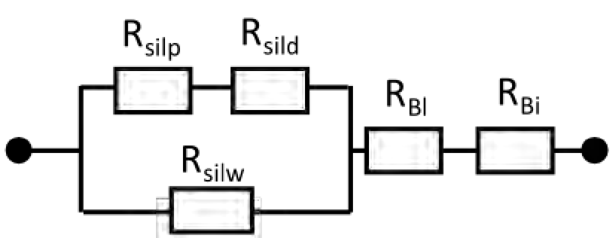


Extraction results using TCAD simulation

method robustness

- comparison with calculated resistance using extracted sheet resistance values of W02 with analytical calculation of R_B [7]





l_E = 5um	l_E = 10um
$R_{silw} = 0.3\Omega$	$R_{silw} = 0.2\Omega$
$R_{sild} = 1.9\Omega$	$R_{sild} = 1.9\Omega$
$R_{silp} = 1.4\Omega$	$R_{silp} = 1.4\Omega$
$R_{lc} = 433\Omega$	$R_{lc} = 433\Omega$
$R_{lw} = 4.1\Omega$	$R_{lw} = 2.0\Omega$
$R_{Bl} = 4.1\Omega$	$R_{Bl} = 2.0\Omega$
➢ $R_{Bx} = 4.4\Omega$	➢ $R_{Bx} = 2.2\Omega$

- good agreement with device simulation

Conclusion

- intrinsic base sheet resistance R_{SBi0} increasing with device generation and process improvements for high speed
  - extraction of extrinsic contributions far from origin hence prone to failure
- further investigation of impact of msmt accuracy and process scalability on existing extraction methods
  - appropriate structure already gives good results, what can be improved
- further improvement of extraction methods for more robust flow
  - to be tested: automatic correction of geometrical information (esp. w_E) using dispersion of measured data from regression analysis to overcome scaling issues

- *a special thanks goes to P. Chevalier and E. Canderle for providing the process split wafers*

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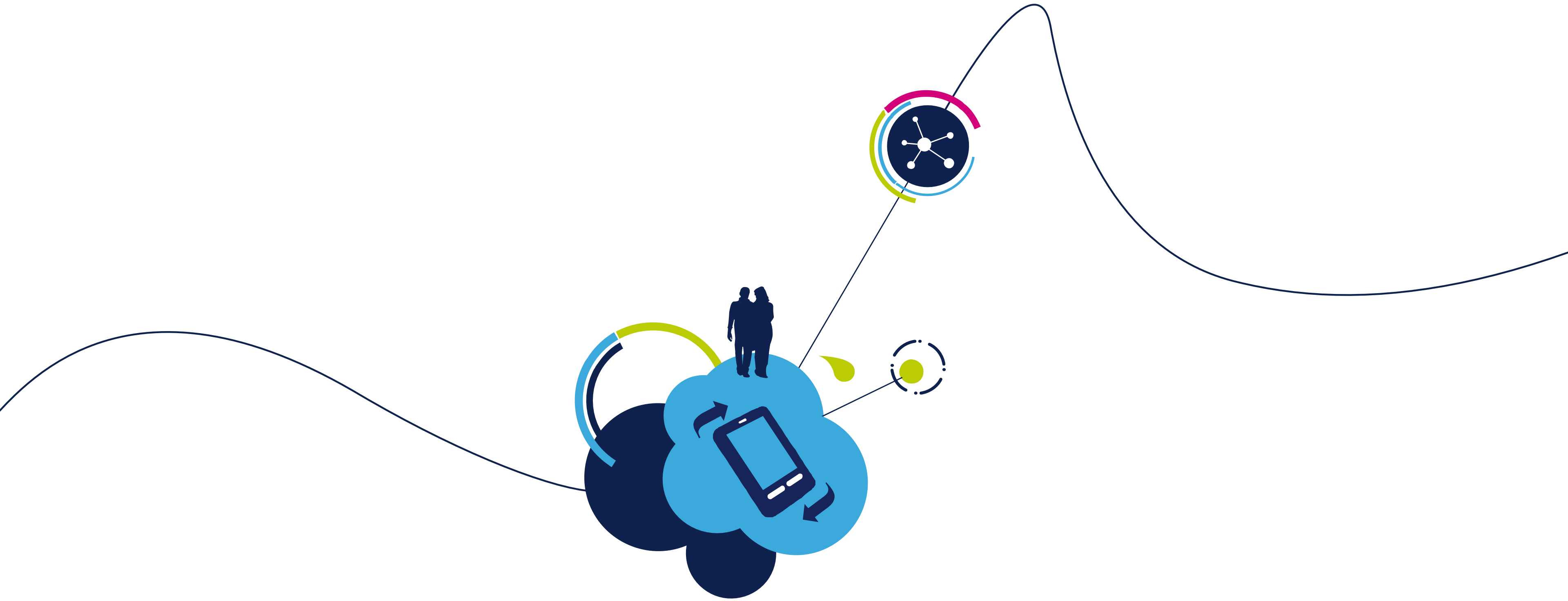

Thank you for your attention!

Literature

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Literature

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